WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

bonding pads;

an input output region surrounding a core region, wherein the input output region comprises input output cells, and wherein a width of the input output cells is approximately equal to or less than a width of the bonding pads; and

core logic arranged within the input output region.

2. The integrated circuit of claim 1, wherein the input output cells are arranged into continuous groups with space between the continuous groups for the core logic.

3. The integrated circuit of claim 1, wherein the core logic occupies a continuous area of the input output region equal to or greater than an area of at least two of the input output cells.

4. The integrated circuit of claim 1, wherein the core logic extends from the core region beyond an outermost boundary of the input output region.

5. The integrated circuit of claim 1, wherein the core logic is further arranged into more than one core logic areas within the input output region.

6. The integrated circuit of claim 1, wherein a width of the core logic is less than a width of the core region.

7. The integrated circuit of claim 1, wherein the input output region comprises four input output sub-regions, wherein each of the four input output sub-regions is arranged proximate a different side of the core region, and wherein a portion of each of the four input output sub-regions comprises the core logic.

8. The integrated circuit of claim 1, wherein the input output cells are arranged on each side of the core region.

9. The integrated circuit of claim 1, wherein the integrated circuit comprises a core limited integrated circuit.

10. The integrated circuit of claim 1, wherein a height of the input output cells is approximately equal to an area sufficient for components of the input output cells divided by the width.

11. The integrated circuit of claim 1, wherein an aspect ratio of the input output cells is greater than about 2.

12. The integrated circuit of claim 1, wherein the bonding pads are arranged in one row spaced from the input output region.

13. The integrated circuit of claim 1, wherein the bonding pads are arranged in first and second rows, and wherein the second row is spaced farther from the input output region that the first row.

14. An integrated circuit, comprising:

four groups of bonding pads, wherein each of the groups of bonding pads is arranged along an axis parallel to a different side of a core region; and

input output sub-regions arranged proximate each of the different sides of the core region, wherein a first portion of each of the input output sub-regions comprises input output cells, and wherein a second portion of each of the input output sub-regions comprises core logic.

15. The integrated circuit of claim 14, wherein a width of the input output cells is approximately equal to or less than a width of the bonding pads.

16. The integrated circuit of claim 14, wherein the integrated circuit comprises a core limited integrated circuit.

17. An integrated circuit, comprising:

a first input output region surrounding a core region, wherein the first input output region comprises first input output cells;

a second input output region surrounding the first input output region, wherein the second input output region comprises second input output cells; and

bonding pads coupled to the first and second input output regions and arranged outside of the first and second input output cells, wherein a width of the first and second input output cells is approximately equal to a pitch of the bonding pads.

18. The integrated circuit of claim 17, wherein the integrated circuit comprises an input output limited integrated circuit.

19. The integrated circuit of claim 17, wherein a height of the first and second input output cells is approximately equal to an area sufficient for components of the first and second input output cells divided by the width.

20. The integrated circuit of claim 17, wherein an aspect ratio of the first and second input output cells is approximately equal to or less than about 0.5.